II. Listing of Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (original) A method for the creation of a suspended inductor, comprising the steps of:

providing a substrate;

creating an inductor in or adjacent to the surface of a layer of dielectric overlying the surface of said substrate;

exposing surface areas of said layer of dielectric; and

etching the exposed surface areas of said layer of dielectric, thereby creating an air gap in said layer of dielectric, said air gap surrounding said inductor.

2. (original) The method of claim 1, said creating an inductor in or adjacent to the surface of a layer of dielectric overlying the surface of said substrate comprising the steps of:

creating a layer of pad oxide over the surface of said substrate;

depositing a layer of dielectric over the surface of said layer of pad oxide;

depositing a layer of etch stop material over the surface of said layer of dielectric;

patterning and etching said layer of etch stop material, thereby creating a pattern of said inductor through the layer of etch stop material;

etching said layer of dielectric to a measurable depth in accordance with said pattern created through said layer of etch stop material, creating a pattern for said inductor in said layer of dielectric; and

filling said pattern created in said layer of dielectric with an inductor material to a measurable height.

3. (original) The method of claim 2, said exposing surface areas of said layer of dielectric further comprising additional steps of:

removing said patterned and etched layer of etch stop material from the surface of said layer of dielectric where said layer of etch stop material aligns with said inductor and overlies a first plane formed by said first upper line of said first cross section of said spirals of said inductor, said first plane further being parallel with the surface of said substrate; and

removing said layer of dielectric where said layer of dielectric aligns with said inductor and overlies said first plane.

4. (original) The method of claim 2, additionally comprising a step of creating at least one supporting pillar for said inductor through said layer of dielectric, said additional step being performed prior to said filling said pattern created in said layer of dielectric with a metal to a measurable height.

5. (original) The method of claim 1, said etching the exposed surface areas of said layer of dielectric comprising exposing said exposed surface areas to an etchant having high etch sensitivity for said layer of dielectric.

6. (original) The method of claim 5, said etchant comprising slope.

7. (original) The method of claim 1, said etching the exposed surface areas of said layer of dielectric comprising using a slope etcher.

8. (original) The method of claim 7, said slope etcher being used under conditions of applying, per liter of slope and contained therein: 107 ml of DIW, 509 ml of BOE diluted in the ratio of 10:1, 35 ml of 49% HF and 349 ml of CH_3OH, applied at a temperature of 25 degrees C. and for the time of 1 minute.

9. (original) The method of claim 4, said step of creating at least one supporting pillar comprising steps of creating patterned and etched overlying layers of semiconductor material, said patterned and etched overlying layers of semiconductor material underlying and being aligned with at least one element of said pattern of said inductor, said patterned and etched overlying layers of semiconductor material having an etch sensitivity when applying a first etchant thereto that is lower than the etch sensitivity of said layer of dielectric when applying said first etchant thereto by a measurable amount.

10. (original) The method of claim 1, said layer of dielectric comprising silicon dioxide, created to a thickness not less than about 5.0 μm.

11. (original) The method of claim 1, said inductor being a spiral inductor.

12. (original) The method of claim 2, said measurable height being about 1.2 μm.

13. (original) The method of claim 9, said patterned and etched overlying layers of semiconductor material comprising material selected from the group consisting of polysilicon and contact pad material and silicon nitride.

14. (original) The method of claim 4, said step of creating at least one supporting pillar comprising steps of creating patterned and etched overlying layers of semiconductor material, said patterned and etched overlying layers of semiconductor material underlying and being aligned with at least one element of said pattern of said inductor, said patterned and etched overlying layers of semiconductor material having an etch sensitivity that is less than an etch sensitivity of an oxide based layer of dielectric by a measurable amount.

15. (original) A method for the creation of a suspended inductor, comprising the steps of:

providing a substrate;

successively depositing over the surface of said substrate a first layer of pad oxide over the surface of which is deposited a second layer of dielectric material over the surface of which is deposited a third layer of etch stop material;

patterning and etching said layer of etch stop material, creating an inductor pattern there-through;

etching to a first measurable depth said layer of dielectric in accordance with said inductor pattern;

filling said etch inductor pattern etched in said layer of dielectric with an inductor material to a second measurable height, said layer of inductor material having an upper surface;

removing said patterned and etched layer of etch stop material and said etched layer of dielectric from above said upper plane of said inductor material where said patterned and etched layer of etch stop material and said etched layer of dielectric align with said inductor, thereby additionally exposing said layer of dielectric; and

exposing said additionally exposed layer of dielectric to an etchant, said etchant having a high ratio between a rate of removal of said layer of dielectric and a rate of removal of said inductor material, thereby removing said exposed layer of dielectric by a measurable amount.

16. (original) The method of claim 15, additionally comprising a step of creating at least one supporting pillar for said inductor through said layer of dielectric, said additional step being performed prior to said filling said etch inductor pattern in said layer of dielectric with an inductor material.

17. (original) The method of claim 15, said etchant comprising slope.

18. (original) The method of claim 15, said exposing said additionally exposed layer of dielectric to an etchant comprising using a slope etcher.

19. (original) The method of claim 18, said slope etcher being used under conditions of applying, per liter of slope and contained therein: 107 ml of DIW, 509 ml of BOE diluted in the ratio of 10:1, 35 ml of 49% HF and 349 ml of CH_3OOH, applied at a temperature of 25 degrees C. and for the time of 1 minute.

20. (original) The method of claim 16, said step of creating at least one supporting pillar comprising steps of creating patterned and etched overlying layers of semiconductor material, said patterned and etched overlying layers of semiconductor material underlying and being aligned with at least one element of said inductor pattern, said patterned and etched overlying layers of semiconductor material having an etch sensitivity when applying a first etchant thereto that compared with an etch sensitivity of said layer of dielectric when applying said first etchant thereto is lower by a measurable amount.

21. (original) The method of claim 15, said layer of dielectric comprising silicon dioxide, created to a thickness not less than about 5.0 μm.

22. (original) The method of claim 15, said second measurable height being about 1.2 μm.

23. (original) The method of claim 20, said patterned and etched overlying layers of semiconductor material comprising material selected from the group consisting of polysilicon and contact pad material and silicon nitride.

24. (original) The method of claim 15, said step of creating at least one supporting pillar comprising steps of creating patterned and etched overlying layers of semiconductor material, said patterned and etched overlying layers of semiconductor material underlying and being aligned with at least one element of said inductor pattern, said patterned and etched overlying layers of semiconductor material having an etch sensitivity that is lower than an etch sensitivity of an oxide based layer of dielectric by a measurable amount.

25. (original) The method of claim 2, said pad oxide comprising silicon dioxide, created to a thickness of about 0.4 μm.

26. (original) The method of claim 15, said first layer of pad oxide comprising silicon dioxide, created to a thickness of about 0.4 μm.

27. (original) The method of claim 2, said layer of etch stop material comprising silicon nitride (Si_3N_4).

28. (original) The method of claim 15, said third layer of etch stop material comprising silicon nitride (Si_3N_4).

29. (withdrawn) A structure for a suspended inductor, comprising:

a substrate;

an inductor on or adjacent to the surface of a layer of dielectric;

at least one supporting pillar having been created for said inductor;

said patterned and etched layer of etch stop material and said etched layer of oxide based dielectric having been removed from above said upper plane of said inductor material where said patterned and etched layer of etch stop material and said etched layer of oxide based dielectric align with said inductor, thereby additionally exposing said layer of oxide based dielectric; and

said additionally exposed layer of oxide based dielectric having been etched using a slope etcher.

30. (withdrawn) The structure of claim 29, said slope etcher having been used under conditions of applying, per liter of slope and contained therein: 107 ml of DIW, 509 ml of BOE diluted in the ratio of 10:1, 35 ml of 49% HF and 349 ml of CH_3OOH, applied at a temperature of 25 degrees C. and for the time of 1 minute.

31. (withdrawn) The structure of claim 29, said at least one supporting pillar comprising patterned and etched overlying layers of semiconductor material, said patterned and etched overlying layers of semiconductor material underlying and being aligned with at least one element of said inductor pattern, said patterned and etched overlying layers of semiconductor material having an etch sensitivity when applying a first etchant thereto that compared with an etch sensitivity of said layer of oxide based dielectric when applying said first etchant thereto is lower by a measurable amount.

32. (withdrawn) The structure of claim 29, said layer of oxide based dielectric having been created to a thickness not less than about 5.0 μm.

33. (withdrawn) The structure of claim 29, said second measurable height being about 1.2 μm.

34. (withdrawn) The structure of claim 29, said first layer of pad oxide comprising silicon dioxide, created to a thickness of about 0.4 μm.

35. (withdrawn) The structure of claim 29, said third layer of etch stop material comprising silicon nitride (Si_3N_4).

36. (withdrawn) A structure for a suspended inductor, comprising:

a substrate;

a first layer of pad oxide deposited over the surface of said substrate of which is deposited a second layer of oxide based dielectric material over the surface of which is deposited a third layer of etch stop material;

said layer of etch stop material having been patterned and etched, creating an inductor pattern there-through;

said layer of oxide based dielectric having been etched to a first measurable depth in accordance with said inductor pattern; then

said etched inductor pattern having been filled with an inductor material to a second measurable height, said layer of inductor material having an upper surface;

said patterned and etched layer of etch stop material and said etched layer of oxide based dielectric having been removed from above said upper plane of said inductor material where said patterned and etched layer of etch stop material and said etched layer of oxide based dielectric align with said inductor, thereby additionally exposing said layer of oxide based dielectric; and

said additionally exposed layer of oxide based dielectric having been etched using a slope etcher.

37. (withdrawn) The structure of claim 36, additionally at least one supporting pillar having been created for said inductor through said layer of oxide based dielectric.

38. (withdrawn) The structure of claim 36, said slope etcher having been used under conditions of applying, per liter of slope and contained therein: 107 ml of DIW, 509 ml of BOE diluted in the ratio of 10:1, 35 ml of 49% HF and 349 ml of CH_3OOH, applied at a temperature of 25 degrees C. and for the time of 1 minute.

39. (withdrawn) The structure of claim 36, said at least one supporting pillar comprising patterned and etched overlying layers of semiconductor material, said patterned and etched overlying layers of semiconductor material underlying and being aligned with at least one element of said inductor pattern, said patterned and etched overlying layers of semiconductor material having an etch sensitivity when applying a first etchant thereto that compared with an etch sensitivity of said layer of oxide based dielectric when applying said first etchant thereto is lower by a measurable amount.

40. (withdrawn) The structure of claim 36, said layer of oxide based dielectric having been created to a thickness not less than about 5.0 μm.

41. (withdrawn) The structure of claim 36, said inductor material comprising TiW/Al-1% Si/TiW.

42. (withdrawn) The structure of claim 36, said second measurable height being about 1.2 μm.

43. (withdrawn) The structure of claim 36, said first layer of pad oxide comprising silicon dioxide, created to a thickness of about 0.4 μm.

44. (withdrawn) The structure of claim 36, said third layer of etch stop material comprising silicon nitride (Si_3N_4).

45. (withdrawn) The structure of claim 37, said at least one supporting pillar comprising patterned and etched overlying layers of semiconductor material, said patterned and etched overlying layers of semiconductor material underlying and being aligned with at least one element of said inductor pattern, said patterned and etched overlying layers of semiconductor material having an etch sensitivity when applying a first etchant thereto that compared with an etch sensitivity of said layer of oxide based dielectric when applying said first etchant thereto is lower by a measurable amount.